Remarks:

Reconsideration of the application is requested.

Claims 1-19 remain in the application. Claims 1, 4, 5, 8, 9, 10, and 14 have been amended. A marked-up version of the claims is attached hereto on separate pages.

In item 1 on page 2 of the above-identified Office Action, claims 1-19 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that it is not clear what is meant by the phrase "intelligent power semiconductor."

An "intelligent power semiconductor" element is the same as a "Smart Power Switch" as indicated on page 11, lines 11-12 of the instant specification. Such elements or components are well-known in the industry as described in the enclosed articles entitled "Power Semiconductor Devices" by Baliga (in particular, note Chapter 10.7, "Smart Power Integrated Circuits") and "Leistungs-MOS-FET-Praxis" by Steng/Tihanyi (in particular, note Chapter 7). Moreover, Webster's Dictionary defines "intelligent" as synonomous with "smart."

Notwithstanding the foregoing, applicant has replaced the term "intelligent power semiconductor" with "**integrated** power semiconductor element" where appropriate throughout the claims. Other changes also have been made to the claims for cosmetic reasons and purposes of clarity.

Support for the change from "intelligent power semiconductor" to "integrated power semiconductor element" is found on page 4, line 8 and page 11, lines 11-12 of the specification of the instant application. Support for clarification that the power switch has a load output and the connection of the load to the load output may be found on page 5, lines 8-9, page 6, lines 21-22, page 11, lines 15-18, as well as in Fig. 2 of the drawings of the instant specification. Support for the "integrated display element" in claim 14 is found on page 8, lines 6-8 of the instant specification.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above noted changes to the claims are provided solely for the purpose of satisfying the requirements of 35 U.S.C. § 112. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In item 4 on page 2 of the above-identified Office Action, claims 1-19 have been rejected as being fully anticipated by Whitmire et al. (U.S. 6,313,751) under 35 U.S.C. § 102(b).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found at the locations mentioned above in the instant specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, an

> **integrated power semiconductor element** having a **single diagnostic output**, a logic element, and **a power switch** for switching a load and having a load output, a current source, and a current sink; the load being connected to said load output, the **current source and the current sink being connected to said single diagnostic output** and providing a current at said diagnostic output; **said logic element controlling at least one of said power switch, and the current source and the current sink.**

The Whitmire et al. reference discloses a battery failure indicator for positively indicating the operating condition of a battery. There is disclosed a LED element 114 having LED's 118, 120. The LED 118 illuminates when the battery fault condition is false and the LED 120 illuminates when the battery condition is

correct. See col. 2, lines 57-61. The reference also discloses a multi-color LED arrangement 150 shown in Fig. 3.

Clearly, Whitmire et al. do not disclose or teach an integrated power semiconductor element having a power switch (preferably a power semiconductor switch in a preferred embodiment), or a single diagnostic output which is connected with a current source or a current sink, or a control logic circuit for controlling at least one of the power switch, the current source, and the current sink, as recited in lines 3-10 of claim 1 of the instant application.

Further, Whitmire et al. do not disclose or teach "a current source and current sink...disposed in a half-bridge configuration...having a center tap ...connected to said single diagnostic output." as recited in dependent claim 5, or the use of MOSFETs as recited in dependent claims 6-8 and 13, or the use of a power semiconductor component as recited in dependent claim 12 of the instant application.

Independent claim 14 is directed to an integrated display element for diagnosing and displaying disturbances in a semiconductor element. The display element has an input terminal for connection to the semiconductor element and also for receipt of a diagnostic signal from the semiconductor element. Whitmire et al. do not disclose an "input terminal" as recited in claim 14, or "light-emitting diodes" that respond to "a disturbance of the

semiconductor element upon receiving the diagnostic signal fed through said input terminal" as recited in claim 14

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 14, as well as the dependent claims for reasons as discussed above. Claims 1 and 14 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 14, and certain of the dependent claims contain limitations that are not shown or suggested in the cited prior art..

In view of the foregoing, reconsideration and allowance of claims 1-19 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

Respectfully submitted,

For Applicant

FDP/tk

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February 26, 2003

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Application No. 09/928,010

Version With Markings to Show Changes Made:

In the Specification:

Paragraph beginning at line 22 of page 2 has been amended as follows:

With the foregoing and other objects in view, there is provided, in accordance with the invention, a circuit configuration. The circuit configuration includes an intelligent power semiconductor having a single diagnostic output <u>and a load output</u>, a logic element, and a power switch. The power switch switches a load, a current source, and a current sink. The load <u>connects to the load output</u>, <u>and</u> the current source, and the current sink connect to a single diagnostic output and provide a current at the diagnostic output. The logic element can control the power switch and/or the current source and the current sink. The circuit configuration also includes a display element having light-emitting semiconductor diodes, a first terminal, and a second terminal. The first terminal electrically connects to the single diagnostic output of the semiconductor element. The second terminal electrically connected to the load output of the power switch. The light-emitting semiconductor diodes connects in antiparallel between the first terminal and the second terminal and outputs different visual information items when receiving different currents.

In the Claims:

Claim 1 (Amended). A circuit configuration, comprising:

an [intelligent] integrated power semiconductor element having a single diagnostic output, a logic element, [and] a power switch for switching a load and having a load output, a current source, and a current sink; the load connected to said load output, the current source[,] and the current sink being connected to [a] said single diagnostic output and providing a current at [the] said diagnostic output; said logic element [for] controlling at least one of said power switch, and the current source and the current sink; and

a display element having [a] light-emitting semiconductor diodes, a first terminal, and a second terminal; said first terminal electrically connected to said single diagnostic output of said integrated power semiconductor element; said second terminal electrically connected to [the] said load output of said power switch; and said light-emitting semiconductor diodes being connected in antiparallel between said first terminal and said second terminal and outputting different visual information items when receiving different currents.

Claim 4 (Amended). The circuit configuration according to claim 2, wherein said integrated power semiconductor element connects to the load.

Claim 5 (Amended). The circuit configuration according to claim 1, wherein the current source and current sink are disposed in a half-bridge configuration relative to one another having a center tap, and the center tap [being] is connected to said single diagnostic output.

Claim 8 (Amended). The circuit configuration according to claim 1, wherein the current [sound] source and the current sink are MOSFETs.

Claim 9 (Amended). The circuit configuration according to claim 1, wherein said [intelligent] integrated power semiconductor element further includes an input terminal, an output terminal connected to the load, and a supply terminal for receiving a supply potential.

Claim 10 (Amended). The circuit configuration according to claim 9, wherein said [intelligent] integrated power semiconductor element is a low-side switch having a single supply terminal, at which a first supply potential is present, and outputting a second supply potential at said output terminal.

Claim 14 (Amended). [A] An integrated display element for diagnosing and displaying a disturbance in [an intelligent power] a semiconductor element , the integrated display element comprising:

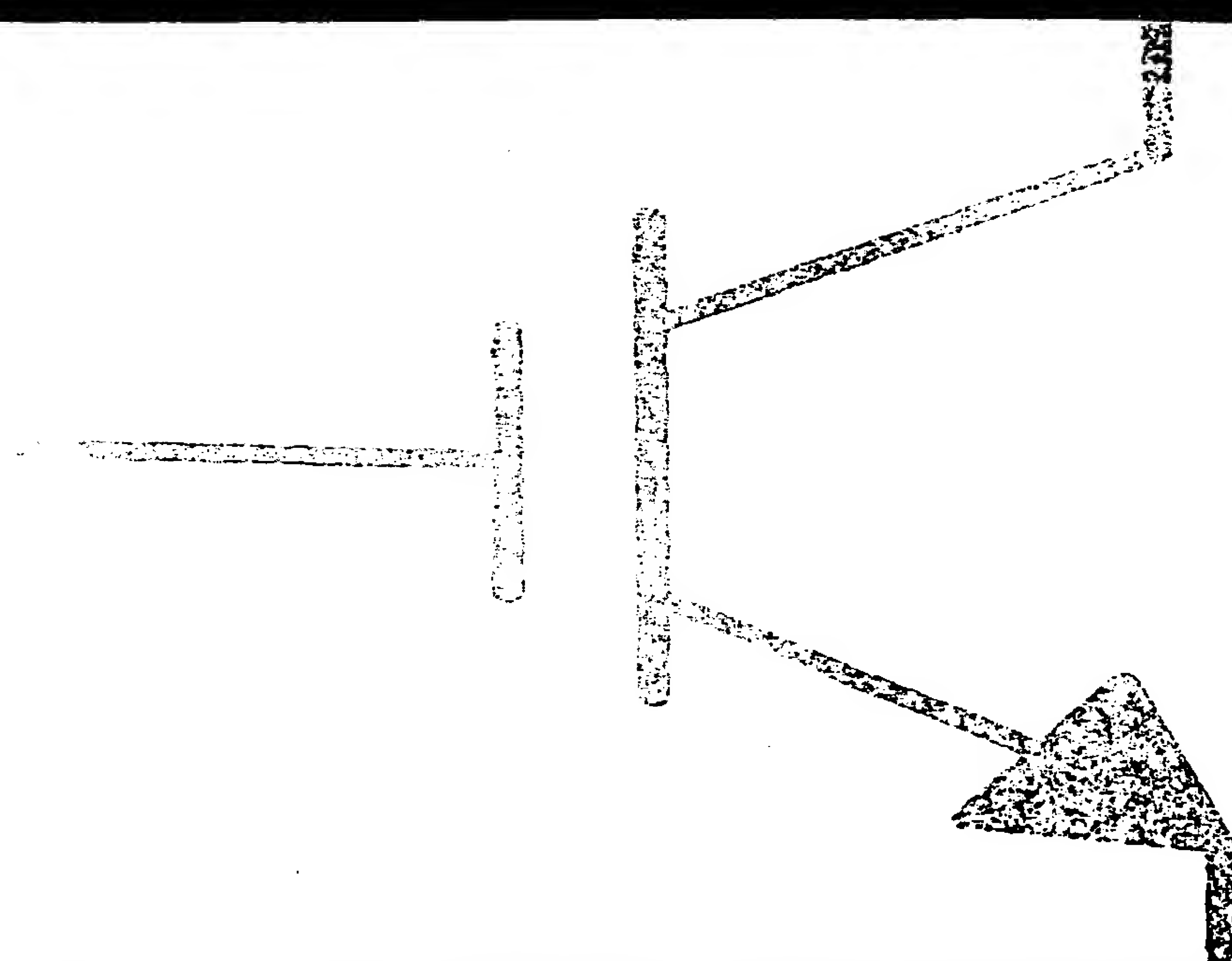
an input terminal for connecting to [an intelligent] the [power] semiconductor element and for receiving a diagnostic signal from the semiconductor element;

a supply terminal for receiving a supply potential; and

light-emitting semiconductor diodes being connected in antiparallel between said input terminal and said supply terminal; said light-emitting semiconductor diodes outputting differing light signals as a function of a disturbance of the [intelligent power] semiconductor element upon receiving [a] the diagnostic signal fed through said input terminal.

POWER SEMICONDUCTOR DEVICES

B. JAYANT BALIGA



POWER SEMICONDUCTOR DEVICES

B. JAYANT BALIGA
North Carolina State University

In this new book, the author provides a chapter-length discussion of each of the following power devices—Power Rectifiers, Power Bipolar Transistors, Power Thyristors, Power MOSFETs, IGBTs, and MOS–Gated Thyristors. In each case, the author introduces the basic structure for the device and its electrical output characteristics, followed by a detailed study of the physics of device operation in the static blocking and current conduction states, and closing with an analysis of the switching behavior including the safe-operating-area. The book's analytical treatment, reinforced by approximately 700 equations, provides a unique insight into the physics of semiconductor power devices.

FEATURES

- *End-of-chapter problem sets, more than 400 figures, and numerous worked-out examples build comprehension of concepts.*
- *Text includes a thorough discussion (in Chapter 3) of the physics of avalanche breakdown and leakage current flow within device structures.*

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10.7 SMART POWER INTEGRATED CIRCUITS

The development of the power MOSFET and IGBT resulted in greatly simplifying the gate drive circuits for motor drive applications. Since the IGBT gate drive circuit has fewer components than the base drive circuit for bipolar transistors and only relatively small currents are needed to control the IGBT, it became possible to integrate the gate drive circuit into a monolithic chip for the first time. This in turn created the opportunity to add other functions, such as protection against adverse operating conditions and logic circuits to interface with microprocessors.

In a three-phase-leg motor drive circuit, it is possible to partition the drive in two basic ways. In one case, all the drive circuits for the lower switches in the totem pole configuration are integrated together on one chip while all the drive circuits for the upper switches in the totem pole configuration are integrated on a second chip. This avoids the need to integrate level shifting capability within the chip but requires a separate high voltage chip for providing this feature. Alternately, the drive can be partitioned with the drive circuits for both the upper and lower switch in each phase leg integrated on a monolithic chip. In order to achieve this capability, technology has been developed to integrate the level-shifting circuits for the upper switch. This also requires the ability for the drive circuit to rise in potential to above the DC bus voltage in order to turn on the upper switch. Three such control chips would be required in a three phase system.

In the smart power control chip, the sensing and protection circuits are usually implemented using analog circuits with high speed bipolar transistors. These circuits must sense the following adverse operating conditions: over-temperature, over-current, over-voltage, and under-voltage. It is obvious that an over-temperature and over-current condition can cause thermal runaway, leading to destructive failure, while an over-voltage condition can lead to avalanche injection induced failure. The under-voltage lockout feature is also necessary because sufficient gate drive voltages are not generated at low bus voltages, leading to very high power dissipation in the output transistors. An example of this condition is during system start-up. The bipolar transistors used in the analog portion must have a high frequency response because of the high dI/dt during short-circuit conditions. When the current exceeds a threshold value, the feedback loop must react in a short duration to prevent the current from rising to destructive levels.

Today's smart power chips are manufactured using a junction isolation technology. In these chips, the high voltage level-shifting transistors are usually lateral structures made using the RESURF principle to obtain a high breakdown voltage with thin epitaxial layers. It is anticipated that dielectric isolation (DI) technology will replace the junction isolation (JI) technology that is now being used for most smart power ICs. Dielectric isolation offers reduced parasitics, a more compact isolation area, and the prospects for integrating MOS-gated bipolar devices that occupy less space than the lateral MOSFETs. A detailed discussion of power integrated circuits is beyond the scope of this book.

Jens Peer Stengl/Jenö Tihanyi

Leistungs-MOS-FET-Praxis

Mit 231 Abbildungen

Pflaum Verlag München

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Inhalt

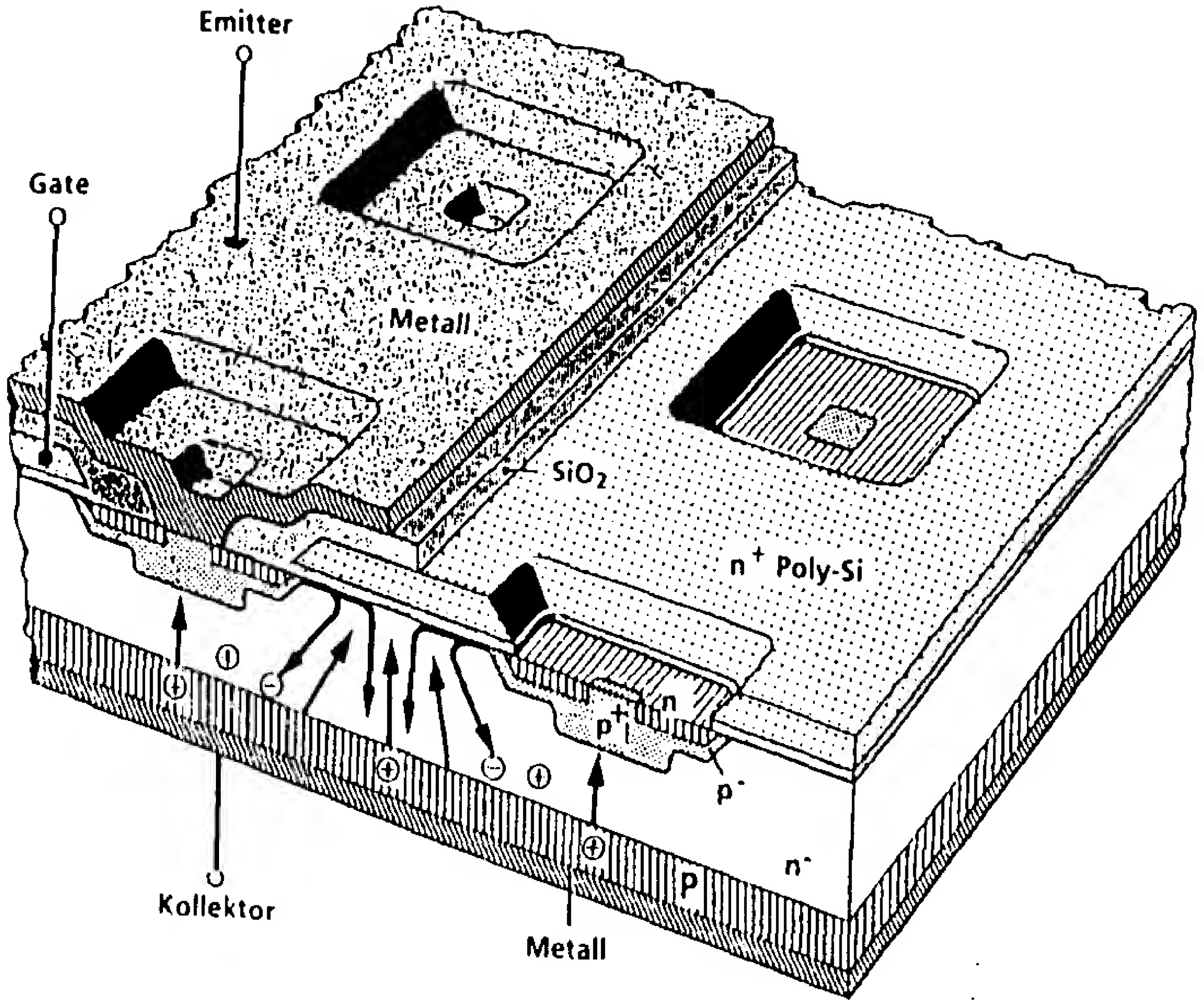

Bild 6.3.3: Querschnitt durch einen IGBT.

kann, ohne außer Kontrolle zu geraten und zerstört zu werden (z. B. Latchen oder Second-Breakdown).

Nach diesem Abstecher zu hohen Spannungen und Strömen wollen wir uns mit neuen, nahezu unzerstörbaren Bauelementen im Bereich <100 V beschäftigen.

7. Intelligente Leistungs-MOS-FETs (SMART-FETs)

Der „SMART-FET", „SMART-POWER-Transistor", „SMART-MOS" oder ... wie auch immer die Bauelemente bezeichnet werden, ist eine neue Generation von Leistungsschaltern, die MOS-Leistung und MOS-Logik in sich vereinen. Sie fügen sich in den Trend der zukünftigen Entwicklungen, wie z. B. Steuerungen mit intelligenter Peripherie ein.

7.1 Eigenschaften intelligenter Leistungs-MOS-FETs

Da Leistungs-MOS-FETs ohne große Steuerleistung betrieben werden können, d. h. auch von MOS-Schaltungen aus, liegt es nahe Ansteuerschaltungen und andere Logikfunktionen gleich in den Leistungsschalter mitzuintegrieren. Die Vorteile eines solchen „intelligenten" Leistungsschalters oder kurz auch SMART-FET sind:

- hohe Zuverlässigkeit gegenüber Schaltungen mit Einzelbauelementen
- Schutzfunktionen, wie Erkennen von Über- und Unterspannung, Überstrom, Kurzschluß (in der Zuleitung oder Last), Leerlauf (Zuleitung oder Last unterbrochen) und Übertemperatur des Bauelementes
- Eingebaute Ladungspumpe für den Betrieb als Highside-Schalter (Source-Folger)
- Klemmen von negativen Spannungsspitzen beim Schalten von induktiven Lasten
- ESD-Schutz an Ein-, und Ausgängen
- Ein-, und Ausgänge CMOS-, bzw. TTL-kompatibel
- Rückmeldung von Zuständen über ein Status-Signal.

Da die Erfassung und Verarbeitung der Daten direkt oder unmittelbar am Leistungs-Chip erfolgt und aufbereitete Meldungen am Status-Ausgang abgefragt werden können, ist eine hohe Sicherheit gegen Störungen gewährleistet. Bauelemente mit eben genannten Eigenschaften werden von verschiede-

nen Herstellern mit unterschiedlichen Funktionen angeboten. Einsatzbereiche sind Leistungsstufen für Mikroprozessor-, oder CMOS-Steuerungen mit Spannungen <60 V. Man findet dies in Industriesteuerungen, programmierbaren Maschinensteuerungen und KFZ-Anwendungen mit Batteriespannungen von 12 V oder 24 V und definierten Spannungsspitzen bis 80 V.
Für die Herstellungsprozesse der Bauelemente wird eine Mischung aus CMOS-Logik-, lateraler bzw. vertikaler Hochspannungs-Logik- und Leistungs-MOS-Technologie verwendet.
Die Herstellung der Bauelemente kann erfolgen als

7.1.1. Monolithisch aufgebaute SMART-FETs

Hier sind Leistungsteil und Logik auf einem Chip vereint (siehe *Bild 7.1.1*). Da der Platz den die Logik beansprucht mit dem Leistungsteil geteilt werden

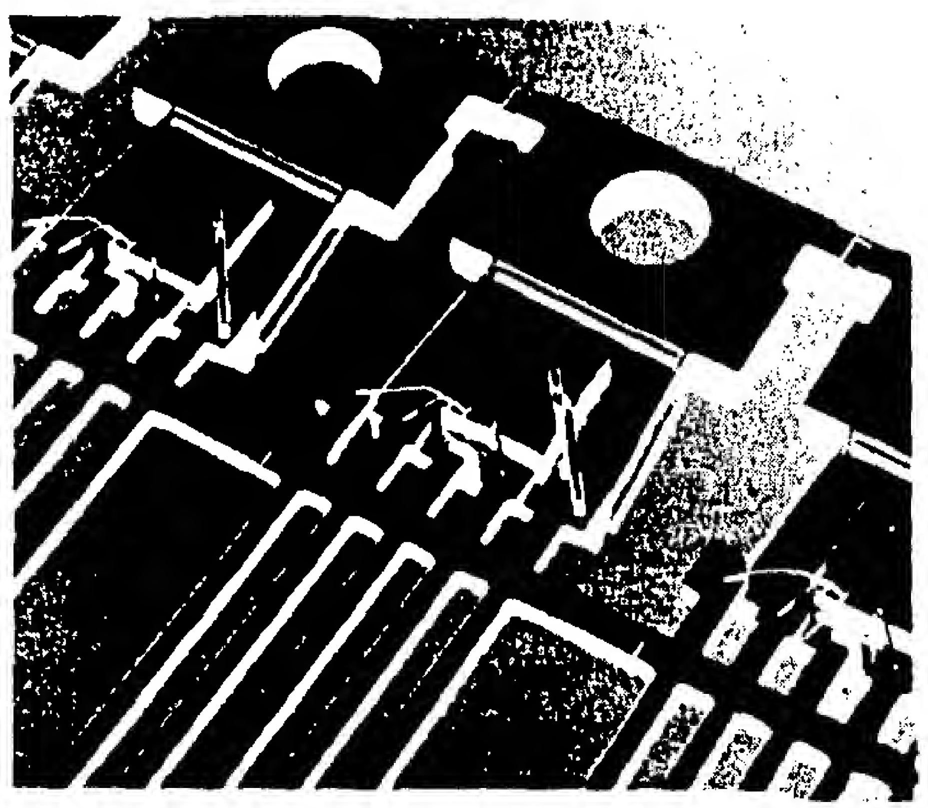

Bild 7.1.1: Montierter Monolythischer SMART-FET im TO-220/5 Gehäuse.

muß, sind nicht so niedrige $R_{DS(on)}$-Werte wie beim MOS-Leistungstransistor gleicher Chipfläche möglich. Je nach angewandter Technologie können Highside-, oder Lowside-Schalter (siehe Kapitel 8.15 Schalten masseseitiger Lasten) auch mit mehreren Ausgängen hergestellt werden.

7.1.2 Chip on Chip SMART-FETs

Auf einem Leistungstransistor-Chip wird ein Logik-Chip montiert, kontaktiert und umpreßt (siehe *Bild 7.1.2* TEMP-FET und *7.1.3* SMART-FET größerer Leistung). Mit der Chip on Chip Technologie ist es möglich, SMART-FETs herzustellen, die in einem TO-220/5 Gehäuse den größtmöglichen Leistungstransistorchip und zusätzlich Logikfunktionen vereinen. Für Leistungsteil und Logik sind jeweils optimale Technologien möglich. Zusätzlich können, sehr einfach, unterschiedliche Leistungs-Chips mit einem Logik-Chip versehen werden.

Bild 7.1.2: Chip on Chip Montage eines TEMP-FET.

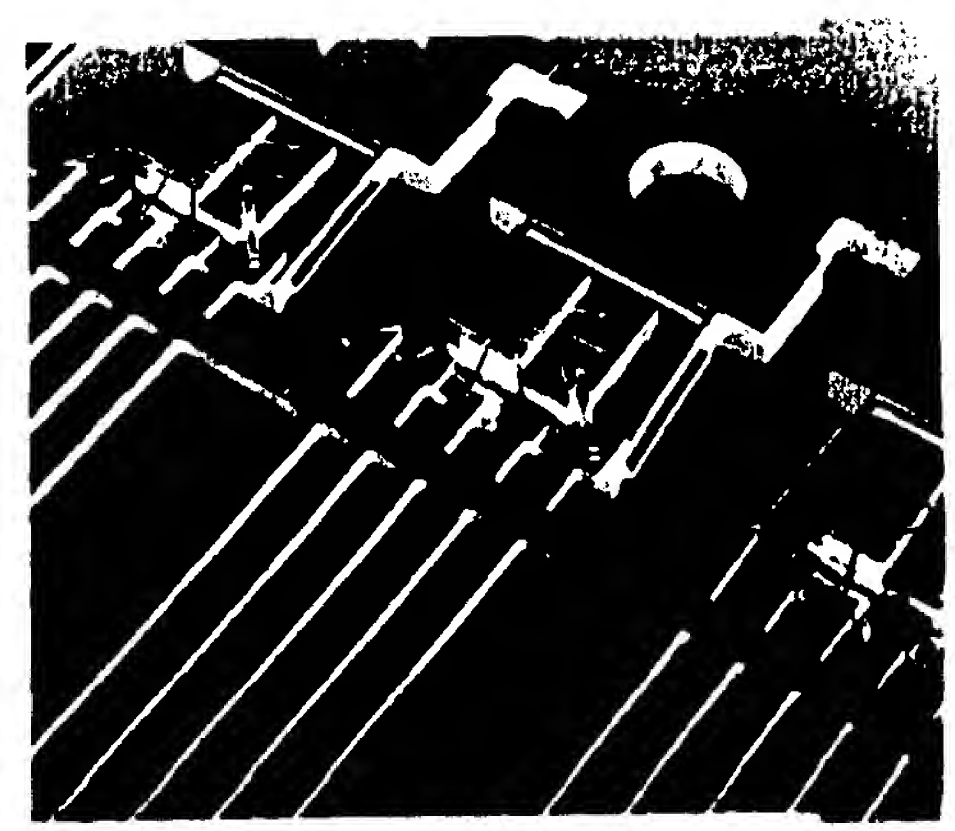

Bild 7.1.3: Chip on Chip Montage eines PRO-FET BTS432.

As for claim 14, we conformed this claim with original German claim 9 as you instructed.

We will keep you advised of any further developments in this application, as they occur.

Very truly yours,

For the Firm

FDP/tk

Encls.: Amendment, Bill